UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/081,818	02/20/2002	Jerome M. Eldridge	1303.045US1	3148

21186 7590 04/29/2005

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402-0938

EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 04/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/081,818	ELDRIDGE ET AL.	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23,85 and 86* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15,18,21-23,85 and 86* is/are rejected.

7)☒ Claim(s) *16,17 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/14/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 03/14/2005 has been entered.

2. The indicated allowability of claims 1-23 and 85-86 are withdrawn in view of the newly discovered reference(s) to Endo U.S. Patent 5,619,051 and in view of new interpretations of the prior art of record. Rejections based on the newly cited reference(s) and on the new interpretations of the prior art of record follow.

Claim Rejections

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. **Claim 1** is rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Lee et al. U.S. Patent Application Publication 2002/0106536 (the '536 publication, cited in a previous office action).

The reference discloses a floating gate transistor (paragraphs [0004] through [0016] and claim 44), comprising:

a first source/drain region and a second source/drain region separated by a channel region in a substrate (all inherent for the floating gate transistor to function);

a floating gate opposing the channel region and separated therefrom by a gate oxide (inherent);

a control gate (inherent) opposing the floating gate; and

wherein the control gate is separated from the floating gate by an asymmetrical low tunnel barrier intergate insulator (the "high-k dielectric layer"14, and where "low" and "insulator" are interpreted broadly, and where the "tunnel barrier" property is interpreted to be inherent as the high-k dielectric layer 14 is a barrier to, for example, electrons tunneling from, for example, from the floating gate to the inherent control gate) formed by multiple atomic layer deposition (ALD) (claim 11 of the reference for the limitation ALD).

Note that although the reference does not explicitly disclose the limitation "asymmetrical" for the low tunnel barrier intergate insulator 14, the low tunnel barrier intergate insulator 14 depicted in, for example, Fig. 1C, which comprises alternating layers of 18 and 20, which are alternating layers of HfO_2 or ZrO_2 and Al_2O_3 (paragraph [0058]), which inherently comprises respective different barrier heights since they are of different materials, appears to positively possesses the limitation "asymmetrical", as sub-layer 18, at one surface of the low tunnel barrier intergate insulator 14, is formed from one of HfO_2 or ZrO_2 and Al_2O_3 , and sub-layer 20, being numbered differently than sub-layer 18 and at the other surface of the low tunnel barrier intergate insulator 14, appears to be formed of another one of HfO_2 or ZrO_2 and Al_2O_3 which is different from the one that forms the sublayer 18, because 20 is not the same as 18. Since the sub-layers at the two opposing surfaces of the low tunnel barrier intergate insulator 14

appear to be formed of different materials, the sub-layers of the different materials, which have different barrier heights, constitute the limitation "asymmetrical".

5. **Claim 1, 3, 4, and 9** are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Endo U.S. Patent 5,619,051 (the '051 patent).

Referring to **claim 1**, the reference discloses a floating gate transistor, comprising:

a first source/drain region (22 or 24, Fig. 5) and a second source/drain region (24 or 22) separated by a channel region (no number) in a substrate (10);

a floating gate (16) opposing the channel region and separated therefrom by a gate oxide (14);

a control gate (20) opposing the floating gate; and

wherein the control gate is separated from the floating gate by an asymmetrical low tunnel barrier intergate insulator (18A, wherein "the dielectric film 18A is formed of a solid solution of two kinds of metal oxides, and the proportions of two metal oxides vary continuously of stepwise from the bottom plane adjacent to the floating gate 16 to the top plane", column 7, lines 1-8, and where "low" is interpreted broadly, and where the "tunnel barrier" property is interpreted to be inherent as the stepwise-graded dielectric layer 18A is a barrier to, for example, electrons tunneling from, for example, from the floating gate to, for example, the control gate).

However, the reference does not explicitly and positively disclose the limitation "asymmetrical" for the low tunnel barrier intergate insulator, and the low tunnel barrier intergate

insulator 18A is formed by a CVD (deposition) process rather than by multiple ALD deposition process as claimed.

Nevertheless, as for the limitation "asymmetrical", the reference discloses that, as noted above, proportions of two metal oxides vary continuously of stepwise from the bottom plane adjacent to the floating gate 16 to the top plane. In other words, at least the portion of the lower surface and the portion of the upper surface of the low tunnel barrier intergate insulator 18A are formed of different mixtures of different metal oxides, thus having different barrier heights, thus meeting the definition of "asymmetrical". See also column 7, last paragraph for an explicit description of a 0.4eV difference in barrier heights between the two surfaces.

As for the limitation CVD as disclosed by the reference and the claimed multiple ALD, since the two processes both appear to result in an asymmetrical low tunnel barrier intergate insulator, the asymmetrical low tunnel barrier intergate insulator formed by multiple ALD is not patently distinguishable from the asymmetrical low tunnel barrier intergate insulator formed by CVD. In addition, according to another doctrine, a process limitation, such as ALD, is considered a non-limitation in a product claim, if, as, or since the process does not result in a difference in structure as compared to prior art.

Referring to **claim 3**, the reference further discloses that that asymmetrical low tunnel barrier intergate insulator includes an asymmetrical transition metal oxide, as $SrTiO_3$ (column 7, lines 9-12) is a transition metal oxide.

Referring to **claim 4**, although the reference's transition metal oxide is formed of a transition metal not the same as one of the claimed transition metals, they are all transition metals, therefore their metal oxides should be functionally equivalent.

Referring to **claim 9**, although the reference does not explicitly discloses that the floating gate transistor is an n-channel type floating gate transistor, one of ordinary skill in the art recognizes that an n-channel type floating gate transistor and a p-channel type floating gate transistor are only different in the dopants (n or p) used.

6. **Claims 10, 11, 14, and 15** are rejected under 35 U.S.C. 103(a) as being unpatentable over Endo U.S. Patent 5,619,051 (the '051 patent) in view of Orlowski et al. U.S. Patent 6,433,382.

Referring to **claim 10**, the '051 patent discloses a non volatile memory cell substantially as claimed and as detailed above including the asymmetrical low tunnel barrier intergate insulator 18A and a first source/drain region (22 or 24) and a second source/drain region (24 or 22) separated by a channel region (no number) in a substrate. The reference further discloses that the asymmetrical low tunnel barrier intergate insulator has a number of small compositional ranges ("the dielectric film 18A is formed of a solid solution of two kinds of metal oxides, and the proportions of two metal oxides vary continuously of stepwise from the bottom plane adjacent to the floating gate 16 to the top plane", column 7, lines 1-8). However, the reference fails to disclose a body region including the channel region and that the body region including the channel region is formed on the first source/drain region. In other words, the reference discloses a "planar" non volatile memory cell instead of a vertical non volatile memory cell as claimed.

Orlowski, in disclosing also a non volatile memory cell including a pair of source/drain regions, a channel region, a floating gate, and a control gate, teaches that vertical non volatile

memory cell offers many advantages over a planar non volatile memory cell such as space saving, improved performance, reduced masking steps, and fully inverted or fully depleted channel regions (column 14, first paragraph). Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to form the reference's non volatile memory cell such that it has a vertical configuration. One would have been motivated to make such a change because a vertical non volatile memory cell offers many advantages over a planar non volatile memory cell such as space saving, improved performance, reduced masking steps, and fully inverted or fully depleted channel regions, as taught by Orlowski.

Referring to **claim 11**, the '051 patent's material ($SrTiO_3$, column 7, lines 9-12) for the asymmetrical low tunnel barrier intergate insulator meets the limitation of the claimed Markush group of materials.

Referring to **claims 14 and 15**, the device of the '051 patent modified in view of Orlowski thus comprises a vertical floating gate (such as 30, Orlowski's Fig. 1 or Fig. 10) along side a body region (22 or 58), and a vertical control gate (32) along side the vertical floating gate.

7. **Claims 5 and 6** are rejected under 35 U.S.C. 103(a) as being unpatentable over Endo U.S. Patent 5,619,051 (the '051 patent) as applied to claim 1 above, and further in view of Eguchi et al. U.S. Patent 5,618,761.

The '051 patent discloses a non volatile memory cell substantially as claimed and as detailed above including the asymmetrical low tunnel barrier intergate insulator 18A. The reference further discloses that the asymmetrical low tunnel barrier intergate insulator is formed of $SrTiO_3$ (column 7, lines 9-12) by a CVD process, meeting the limitation of the claimed

Markush group of materials of claim 6. The reference further discloses that the asymmetrical low tunnel barrier intergate insulator ought to have a high dielectric constant (the table in column 6, lines 35-45, and claim 1). However, the reference fails to mention the limitation "Perovskite" for the asymmetrical low tunnel barrier intergate insulator.

Eguchi, in disclosing an insulator layer for a capacitor, mentions that a layer comprising Sr, Ti, and O formed by CVD process, has a perovskite crystal structure, which offers a high dielectric constant and excellent insulating properties (column 9, lines 37-45). Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to form the '051 patent's asymmetrical oxide tunnel barrier intergate insulator such that it is an asymmetrical Perovskite oxide tunnel barrier intergate insulator. One would have been motivated to make such a change because perovskite crystal structure offers a high dielectric constant and excellent insulating properties, which high dielectric constant property is desired by the '051 patent and which is taught by Eguchi.

8. **Claims 7-8, 12-13, and 18** are rejected under 35 U.S.C. 103(a) as being unpatentable over Endo U.S. Patent 5,619,051 (the '051 patent).

The '051 patent discloses a non volatile memory cell substantially as claimed and as detailed above for claims 1 and 10 including the asymmetrical low tunnel barrier intergate insulator 18A including a number of small compositional ranges arranged in a "vary continuously of stepwise" from the bottom surface to the top surface. The reference further discloses, in reference to **claim 18**, that the number of small compositional ranges is formed such that gradients can be formed in an applied electric field which produce different barrier heights at

an interface with the floating gate and control gate (paragraph bridging columns 7 and 8, particularly "...gradient of conduction band to make an about 0.4 eV difference...information charge retention time is about twice that in the memory cell of FIG. 1...the erase time shortens to 1/5 of that in the memory cell having the dielectric film 18 of homogeneous barium strontium titanate).

The reference further teaches that the floating gate includes a polysilicon floating gate having a metal silicide formed thereon (column 3, lines 56-63) in contact with the asymmetrical low tunnel barrier intergate insulator, and that the control gate includes a metal control gate having a metal oxide layer formed thereon in contact with the asymmetrical low tunnel barrier intergate insulator.

Compared with the claims, the reference discloses a metal silicide instead of the claimed first metal layer for the floating gate, a metal oxide/metal instead of the claimed second metal/polysilicon for the control gate. However, the differences are deemed to be obvious to one of ordinary skill in the art at the time the invention was made ("the artisan") because at least one of the following two reasons: (1) the materials are known and available to the artisan; (2) both the present invention and the reference fails to show an advantage of one combination of materials to the other.

With respect to the limitation "wherein the metal layer includes a metal layer that has a different work function than the metal layer formed on the floating gate", the limitation appears to be inherent in the reference because: (1) the metal of the metal silicide (functionally equivalent to the claimed first metal) and the metal of the metal oxide (functionally equivalent to the claimed second metal) are different metals, resulting in different work functions; (2) the

paragraph bridging columns 7 and 8, as noted above, expressly states that the barrier heights at the two surfaces of the asymmetrical low tunnel barrier intergate insulator, where the metal silicide and the metal oxide are respectively in contact with, ought to be different, leading the artisan to conclude that the work function of the metal silicide (functionally equivalent to the claimed first metal) should be different from the work function of the metal oxide (functionally equivalent to the claimed second metal).

9. **Claim 23** is rejected under 35 U.S.C. 103(a) as being unpatentable over Endo U.S. Patent 5,619,051 (the '051 patent) as applied above for claim 18 and further in view of Orlowski et al. U.S. Patent 6,433,382.

Similarly as detailed above in paragraph numbered 6, the artisan would be motivated to forms the floating gate transistor such that it includes a vertical floating gate transistor.

10. **Claims 10, 11, 14, and 15** are rejected under 35 U.S.C. 103(a) as being unpatentable over Endo U.S. Patent 5,619,051 (the '051 patent) in view of Shinkawata et al. U.S. Patent Application Publication 20020008324.

Referring to **claims 2, 20-22, and 85-86**, the '051 patent discloses a non volatile memory cell substantially as claimed and as detailed above for claims 1, 6, 10, and 18 including the asymmetrical low tunnel barrier intergate insulator 18A including a number of small compositional ranges arranged in a "vary continuously of stepwise" from the bottom surface to the top surface, and wherein the number of small compositional ranges arranged in a "vary continuously of stepwise" includes $SrTiO_3$ (column 7, lines 1-12). The materials for the second

metal (in reference to claims 20 and 21) should also be known and available to the artisan as noted above.

However, instead of the claimed aluminum oxide (Al_2O_3), as noted, the reference discloses $SrTiO_3$.

Shinkawata, in disclosing a gate insulating film 24 for semiconductor device, teaches that the two materials are equivalent (paragraph [0063]) (and they should be because otherwise the claimed device of claims 6, 11, 20-22, which contains both materials, would be inoperable).

Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to form the '051 patent's asymmetrical low tunnel barrier intergate insulator such that it includes aluminum oxide (Al_2O_3) instead of $SrTiO_3$. One would certainly be motivated to do that as a free choice of available and equivalent materials.

Allowable Subject Matter

11. Claims 16-17 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for the indication of allowable subject matter: The cited art, whether taken singularly or in combination, especially when all limitations are considered within the claimed specific combination, fails to teach or render obvious a non-volatile memory cell having all exclusive limitations as recited in claims 10/16 (claims 10 and 16) and claims 18/19, characterized in the limitations of claims 16 and 19 respectively.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Tu-Tu Ho
April 22, 2005